REMARKS

Applicants have reviewed the Office Action dated March 17, 2008, and the references cited therein. Claims 1-6, 8-14, and 16-29 are presently pending. Applicants have amended the claims in response to: the objections to informalities in claims 1, 8, 13, 14 and 23; and the rejection of claims 1-29 under 35 U.S.C. §112 as being indefinite for failing to particularly point out and distinctly claim the invention.

Applicants have amended claim 24 to clarify that *each* single processing element is capable of executing a VLIW instruction. The clarifying amendment is supported by Applicants' description at page 4, lines 13-15, and page 4, line 23 to page 5, line 17 (describing a single processing element including five issue slots and six FU's for processing a VLIW).

Applicants have also amended the presently pending independent claims 1 and 29 to more clearly distinguish their invention from Gove et al. U.S. Pat. No. 5,212,777 (Gove), upon which the prior art-based rejections are primarily based. In particular, claim 1 has been amended (incorporating the recited elements of now-canceled claims 7 and 15) to emphasize that Applicants' invention includes a "reconfigurable channel infrastructure" comprising "a control chain with combination elements for each processing element and a switch between each pair of neighboring processing elements." Applicants' amendments to claim 1 (and 29) are supported by Applicants' specification (see, Applicants' Figs. 3-7 and corresponding written description). In particular, Figs. 5 and 7 and their written description in the specification illustrate the control chain and how switches between neighboring processing elements inhibit transmission of intermediate controls signals (e.g., L1 and L2 in Fig. 5) to a preceding or a succeeding neighboring processing element (PE). Applicants' claimed control chain, placement of switches between processing elements, and more generally, Applicants' presently recited *reconfigurable channel infrastructure connected to the processing elements* is neither disclosed nor suggested by Gove.

Applicants have also amended claim 27 to more particularly recite that the internal interconnect network serves to connect issue slots of the processing elements. See, Fig. 2 interconnect network IN coupled to issue slots IS1-IS5.

Applicants respectfully request reconsideration of each and every ground of rejection set forth in the Office Action in view of Applicants' amendments and remarks provided herein. Please charge any fee deficiencies to Deposit Account No. 12-1216.

Summary of Prior Art-Based Rejections

1. Claims 1-8, 12-15, 18-22, and 24-28**(29)** are rejected under 35 U.S.C. § 102(b) as being anticipated by Gove et al., U.S. Pat. No. 5,212,777 (hereinafter "Gove").

2. Claims 9-11 and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gove in view of Belton's *Basic Gate and Functions* website (hereinafter "Belton").

3. Claims 6 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gove in view of Parcerisa et al.'s *Efficient Interconnects for Clustered Microarchitectures* publication (hereinafter "Parcerisa").

Applicants traverse the grounds for each prior art-based rejection in view of Applicants' amendments and the reasons set forth herein below. Applicants address the specific rejections in the order they arise in the Office Action.

1. Rejection of Claims 1-8, 12-15, 18-22 and 24-28(29) as Anticipated by Gove

Applicants traverse the rejection of **claims 1-8, 12-15, 18-22, and 24-28(29)** as anticipated by Gove since Gove does not disclose or suggest, to one skilled in the art, Applicants' "reconfigurable channel infrastructure" recited in the presently amended claims 1. Amended claim 1 now recites that processing elements are coupled together using a reconfigurable channel infrastructure including: (1) a control chain with combination elements for each processing element and (2) a switch between each pair of neighboring processing elements to controllably inhibit transmission of intermediate control signals (e.g., L1, L2, etc. in Figs. 5 and 6) to a neighboring element.

Applicants' claimed invention

According to the invention recited in independent claim 1, the processing elements are coupled by a reconfigurable channel infrastructure that includes a control chain with combination elements (e.g., combination elements "c" in Fig. 5) for each processing element (e.g., processing

element PE in Fig. 5) and a switch (e.g., switch SW in Fig. 5) between each pair of neighboring processing elements. The switch controllably inhibits transmission of intermediate control signals (e.g., L1 and L2 in Fig. 5) to a neighboring processing element.

The recited invention facilitates providing a dynamically reconfigurable parallel processor at any scale. For example, the processing apparatus as shown in FIG. 5, for which two processing elements are shown, can be extended to multiple times more units by extending the control chain (CHN). The same extension of processing system is enabled by extending the control chain disclosed, by way of both general and specific examples, in the written description.

Thus, in the recited invention, a plurality of processing elements can be dynamically configured via the control chain (CHN) to operate under a common thread of control. It is further noted that, in the claimed dynamically reconfigurable multiprocessor arrangement, a cluster of processing elements is defined by cluster boundaries. For example, in Figure 5, by configuring a first switch before a processing element PE_n, and a second switch after a processing element PE_m coupled to the control chain as non-transmitting, any intermediate cluster control signal will not be exchanged/passed by these two switches to the defined chain. Thus, the set of processing elements N, N+1, N+2, ..., M-1, M forms a cluster that operates independently from the processing elements beyond the switches that are coupled to either end of the configured processing element cluster.

Gove's Disclosed Multiprocessor System

Gove discloses a multiprocessor system that includes a single bus structure connecting a set of processing elements. Gove's disclosed multiprocessor includes four primary components: (1) processors, (2) a cross-bar switch 20, (3) memory cells containing instructions and data, and (4) **a synchronization control bus 40 that carries control signals for programming and executing the synchronization statuses of the processors**. *See*, Gove, FIGs. 1, 4 and 22.

Gove utilizes a universal bus hardware arrangement to control sharing of data/control between processors. In particular, each processor includes a synch control register indicating the processors with which the processor should be synchronized (for data and/or instructions), and each processor has, for each of the other processors, a respective NAND gate connected to the

respective signal line and the respective bit for the other processors. In the Gove arrangement where each processor-to-processor element communication path is direct, the number of control bus lines 40 increases linearly with the increase in the number of processing elements. Moreover, the number of configuration bits increases with the *square* of the number of processing elements.

Thus, in summary, Gove's cross-bar switch connects categorized (grouped) processors with the appropriate memory cells. *See*, Gove, col. 2 lines 47-53. As shown in FIGs. 4 and 22, Gove provides a continuous set of synchronization control signal lines 40 to which synchronization control logic for *each* processing element is connected *in parallel*.

Gove's Processor Architecture Disclosure Does Not Anticipate Applicants' Claims

Gove does not disclose Applicants' claimed multiprocessor system recited in claim 1. The claimed invention includes a reconfigurable channel infrastructure comprising a *control chain* which cannot be found anywhere in Gove. Furthermore, claim 1 now recites the control chain includes a *switch between neighboring processors that locally controllably inhibits transmission of intermediate control signals to a preceding or succeeding processing element in the control chain*. In the multi-processor synchronization control scheme depicted in FIG. 22 of Gove, the NAND gates associated with particular ones of the processing elements cannot inhibit transmission of the synch control signals on synchronization lines 40 to neighboring processing elements.

Gove's universal control bus architecture is the antithesis of Applicants' claimed invention. Gove's "cross-bar switch" based cluster control architecture includes a universal bus and a set of individual direct-connect logic circuits to match processors with instructions located in memory to achieve clustering. In contrast, Applicants' claimed invention includes a reconfigurable channel infrastructure comprising a *control chain* (communicatively connected to the 2D grid of processing elements as shown in Applicants' FIG. 7) that sends controls signals via intermediate paths between serially connected links to the processing elements to achieve clustering.

Moreover, Gove's configurable cluster control logic/circuitry does not include *switches* inserted between, and controlling passage of intermediate cluster control signals between

neighboring processing elements. The recited switches, interposed on the control chain between neighboring processing elements, serve the essential functionality of determining when to transmit intermediate control signals to processing elements attached to the control chain.

In summary, Gove implements multiprocessor cluster control in a way that substantially differs from the recited cluster control hardware recited in claim 1. Gove discloses universal bus-based cluster control logic. Nowhere does Gove disclose or even remotely suggest Applicants' recited control chain including a set of switches implementing localized serial cluster control of a set of processing elements. While both Gove and Applicants' disclosed/claimed cluster control hardware facilitate flexibly cluster processing elements, Gove achieves clustering via a cross-bar switch wherein each processor is provided with individual direct connections to a universal set of cluster control signal lines. Meanwhile, Applicants' claimed reconfigurable channel infrastructure includes a *control chain* for passing cluster signals to the processing elements via switches capable of locally inhibiting transmission of intermediate cluster control signals to neighboring links of the control chain.

Claim 29 is similarly distinguishable from Gove's disclosed cluster control hardware. Claim 29 recites "combining" and "deriving" steps including limitations directed to control chain-based (including using *two or more intermediate control signals*) propagation of cluster control signals for a set of processing elements through the use of intermediate control signals. Gove does not disclose at least the recited intermediate control signals to derive a cluster control signal for processing system including a plurality of processing elements.

Specific Traversals of Anticipation Rejections of Dependent Claims Based on Gove

Claims 2-8, 12-15, 18-22, and 24-28, which depend from independent claim 1, are patentable over Gove for at least the same reasons as claim 1. Furthermore, **claims 2, 6-7, 12-15, 24, and 28** are patentable on independent grounds, as described below.

Applicants traverse the rejection of **claim 2** because Gove does not disclose that processing elements organized in a task unit share at least one common control signal for *controlling instruction execution*. The SYNC'D signals, to which item 24 of the Office Action refers, are not control signals to control instruction execution. Instead the SYNC'D signals

synchronize processors engaged in a same task. The SYNC'D signals are not common to each processing unit since each processing unit receives a separate SYNC'D signal. *See*, Gove, FIG. 22; col.20, ll.17-27. When Gove's invention is in SIMD mode, the processing elements fetch from the same instruction memory, but this is distinct from sharing a common control signal.

With respect to the Office Action's rejection of **claim 6**, Gove does not disclose that data-path connections (DPC) are limited to neighbor-to-neighbor connections. Gove instead discloses that, via the SYNC'D line, every processor is connected to every other processor. *See*, Gove, FIG. 22; col.20, ll.17-27. Furthermore, item 54 of the Office Action states "Gove does not explicitly disclose that the data-path connections are limited to neighbour-to-neighbour connections." This statement appears to contradict the current anticipation rejection of claim 6.

With respect to the Office Action's rejection of **claim 7**, Gove does not disclose "the common control signal is derived from intermediate control signals transmitted through a reconfigurable channel infrastructure connected to the processing elements." Gove does not disclose a *common control signal* since not all processing elements output or receive the same execution signal. Rather each processing unit contains control logic that produces its own unique control signal. *See,* Gove, FIG. 22. Applicants note that this element has been incorporated into **claim 1** and is therefore canceled.

With respect to rejection of **claims 12-14**, Gove does not disclose a "channel infrastructure [comprising] mutually transverse chains." As defined by Applicants' specification and drawings, "transverse chains" correspond to the vertical and horizontal control chains that, aside from their path orientation, are otherwise equivalent. In the Application of Gove to claims 12-14, the Office Action identifies a horizontal chain corresponding to a SYNC line connecting all processors. The vertical lines and associated circuits (i.e., NAND gates and sync control registers) drawn from the horizontal SYNC line cannot correspond to transverse chains since there is no identifiable series of consecutive identical elements.

With respect to rejection of **claim 15**, Gove does not disclose switches between pairs of processing elements for locally controllably inhibiting transmission of intermediate control signals. Gove's NAND gates are not located *between* pairs of processing elements – they are instead located *within* each processing element. *See*, Gove, FIG. 21 in conjunction with Gove,

FIG. 22. Furthermore, the sync control signals in Gove, FIG. 22 do not inhibit transmission of the claimed intermediate signals, but merely synchronize processors running the same instructions. *See,* Gove, col.20, ll.17-27. Applicants note that this element has been incorporated into **claim 1** and is therefore canceled.

With respect to rejection of **claim 24**, given the amendment to claim 24, Gove does not disclose processing elements comprising VLIW processors. While, Gove does disclose that processors may be configured in various modes (Gove, col.62, ll.40-52), Gove does not disclose that each individual processor is a VLIW processor, capable of executing VLIW instructions as recited in claim 24.

With respect to rejection of **claim 28**, Gove does not disclose processing elements arranged in a 2-dimensional grid. Gove discloses a bus structure, with all processing elements along one line connected to the cross-bar switch. *See,* Gove, FIG. 1. Gove, FIG. 22, does not show any 2-dimensional grid system, with processors arranged in a grid. Gove, FIGs. 59-64, which show all possible arrangements of processors, fail to disclose any variation from the one-dimensional bus structure.

Rejection of Claims 9-11 and 16-17 As Obvious Over Gove In View of Belton

Applicants respectfully traverse the rejection of **claims 9-11 and 16-17** under 35 U.S.C. § 103(a) as being unpatentable over Gove in further view of Belton. Claims 9-11 and 16-17 depend on independent claim 1. It is respectfully submitted that such dependent claims are patentable for at least the reasons set forth in Applicants' remarks addressing the rejection of independent claim 1.

Rejection of Claims 6 and 28 As Obvious Over Gove In View of Parcerisa

Applicants respectfully traverse the rejection of **claims 6 and 28** under 35 U.S.C. § 103(a) as being unpatentable over Gove in further view of Parcerisa. Claims 6 and 28 depend on independent claim 1. It is respectfully submitted that such dependent claims are patentable for at least the reasons set forth in Applicants' remarks addressing the rejection of independent claim 1.

Conclusion

Applicants respectfully submit that the patent application is in condition for allowance. If, in the opinion of the Examiner, a telephone conference would expedite the prosecution of the subject application, the Examiner is invited to call the undersigned attorney.

Respectfully submitted,

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Date: September 17, 2008